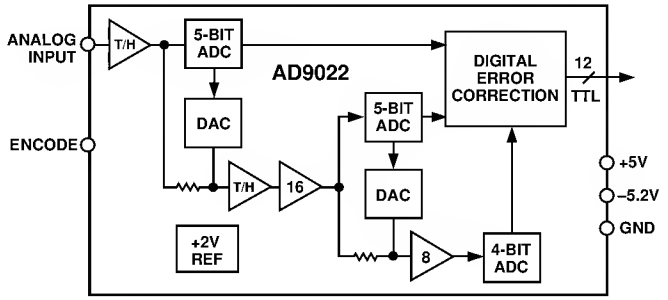
12-Bit 20 MSPS Monolithic A/D Converter

AD9022

FEATURES
Monolithic
12-Bit 20 MSPS A/D Converter
Low Power Dissipation: 1.4 Watts
On-Chip T/H and Reference
High Spurious-Free Dynamic Range
TTL Logic

APPLICATIONS
Radar Receivers
Digital Communications
Digital Instrumentation
Electro-Optics

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9022 is a high speed, high performance, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference, are included on-chip to provide a complete conversion solution. It is a companion unit to the AD9023; the primary difference between the two is that all logic for the AD9022 is TTL-compatible, while the AD9023 utilizes ECL logic for digital inputs and outputs. Pinouts for the two parts are nearly identical.

Operating from +5 V and –5.2 V supplies, the AD9022 provides excellent dynamic performance. Sampling at 20 MSPS with A_{IN} = 1 MHz, the spurious-free dynamic range (SFDR) is typically 76 dB; with A_{IN} = 9.6 MHz, SFDR is 74 dB. SNR is typically 65 dB.

The onboard T/H has a 110 MHz bandwidth and, more importantly, is designed to provide excellent dynamic performance for analog input frequencies above Nyquist. This feature is necessary in many undersampling signal processing applications, such as in direct IF-to-digital conversion.

To maintain dynamic performance at higher IFs, monolithic RF track-and-holds (such as the AD9100 and AD9101 Samplifier™) can be used with the AD9022 to process signals up to and beyond 70 MHz.

With DNL typically less than 0.5 LSB and 20 ns transient response settling time, the AD9022 provides excellent results when low-frequency analog inputs must be oversampled (such as CCD digitization). The full scale analog input is ±1 V with a 300 Ω input impedance. The analog input can be driven directly from the signal source, or can be buffered by the AD96xx series of low noise, low distortion buffer amplifiers.

All timing is internal to the AD9022; the clock signal initiates the conversion cycle. For best results, the encode command should contain as little jitter as possible. High speed layout practices must be followed to ensure optimum A/D performance.

The AD9022 is built on a trench isolated bipolar process and utilizes an innovative multipass architecture (see the block diagram). The unit is packaged in 28-lead ceramic DIPs and gullwing surface mount packages. The AD9022 is specified to operate over the industrial (–25°C to +85°C) and military (–55°C to +125°C) temperature ranges.

Samplifier is a trademark of Analog Devices, Inc.

REV. B

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AD9022- SPECIFICATIONS

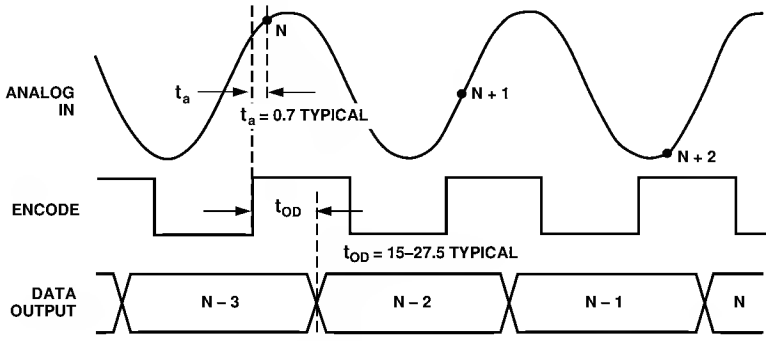
ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = -5.2 V; Encode = 20 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9022AQ/AZ Min	Typ	Max	AD9022BQ/BZ Min	Typ	Max	AD9022SQ/SZ Min	Typ	Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.6	0.75		0.4	0.5		0.6	0.75	LSB
	Full	VI			1.0			1.0			1.0	LSB
Integral Nonlinearity	+25°C	I		1.3	2.5		1.3	2.0		1.3	2.5	LSB
	Full	VI		1.6	3.0		1.6	3.0		1.6	3.0	LSB
No Missing Codes	Full	VI	Guaranteed			Guaranteed			Guaranteed			
Offset Error	+25°C	I		5	25		5	25		5	25	mV
	Full	VI		15	35		15	35		15	35	mV
Gain Error	+25°C	I		0.5	2.5		0.5	2.5		0.5	2.5	% FS
	Full	VI		0.6	3.5		0.6	3.5		0.6	3.5	% FS
Thermal Noise	+25°C	V		0.57			0.57			0.57		LSB, rms
ANALOG INPUT												
Input Voltage Range				±1.024			±1.024			±1.024		V
Input Resistance	Full	IV	240	300	360	240	300	360	240	300	360	Ω
Input Capacitance	+25°C	V		5			5			5		pF
Analog Bandwidth	+25°C	V		110			110			110		MHz
SWITCHING PERFORMANCE[1]												
Minimum Conversion Rate	+25°C	IV			4			4			4	MSPS
Maximum Conversion Rate	Full	VI	20			20			20			MSPS
Aperture Delay (t_A)	+25°C	IV	0.55	0.71	0.85	0.55	0.71	0.85	0.55	0.71	0.85	ns
Aperture Uncertainty (Jitter)	+25°C	V		6			6			6		ps, rms
Output Delay (t_{OD})	Full	VI	15		27.5	15		27.5	15		27.5	ns
ENCODE INPUT												
Logic Compatibility				TTL			TTL			TTL		
Logic "1" Voltage	Full	VI	2.0			2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8			0.8	V
Logic "1" Current	Full	VI		8	20		8	20		8	20	µA
Logic "0" Current	Full	VI		8	20		8	20		8	20	µA
Input Capacitance	+25°C	V		6			6			6		pF
Pulsewidth (High)	+25°C	IV	22.5		125	22.5		125	22.5		125	ns
Pulsewidth (Low)	+25°C	IV	20		125	20		125	20		125	ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	V		20			20			20		ns
Overvoltage Recovery Time	+25°C	V		20			20			20		ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	65	73		70	75		65	73		dBc
@ 1.2 MHz	Full	V		70			72			70		dBc
@ 4.3 MHz	+25°C	V		73			75			73		dBc
@ 9.6 MHz	+25°C	I	63	72		69	74		63	72		dBc
@ 9.6 MHz	Full	V		68			72			68		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	62	64		64	66		62	64		dB
@ 1.2 MHz	Full	V		63			65			63		dB
@ 4.3 MHz	+25°C	V		64			66			64		dB
@ 9.6 MHz	+25°C	I	61	63		63	65		61	63		dB
@ 9.6 MHz	Full	V		62			63			62		dB
Signal-to-Noise Ratio[2] (Without Harmonics)												
Analog Input @ 1.2 MHz	+25°C	I	63	66		65	67		63	66		dB
@ 1.2 MHz	Full	V		64			66			64		dB
@ 4.3 MHz	+25°C	V		66			66			66		dB
@ 9.6 MHz	+25°C	I	62	65		64	66		62	65		dB
@ 9.6 MHz	Full	V		63			65			63		dB

Parameter (Conditions)	Temp	Test Level	AD9022AQ/AZ Min	Typ	Max	AD9022BQ/BZ Min	Typ	Max	AD9022SQ/SZ Min	Typ	Max	Units
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V		74			74			74		dBc
DIGITAL OUTPUTS[1]												
Logic Compatibility				TTL			TTL			TTL		
Logic "1" Voltage	Full	VI	2.4			2.4			2.4			V
Logic "0" Voltage	Full	VI			0.5			0.5			0.5	V
Output Coding				Offset Binary			Offset Binary			Offset Binary		
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Current	Full	VI		100	120		100	120		100	120	mA
$-V_S$ Supply Voltage	Full	VI	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	mA
$-V_S$ Supply Current	Full	VI		180	220		180	220		180	220	mA
Power Dissipation	Full	VI		1.4	1.9		1.4	1.9		1.4	1.9	W
Power Supply Rejection Ratio (PSRR)[4]	Full	V		32			32			32		mV/V

NOTES
[1]AD9022 load is a single LS latch.
[2]RMS signal-to-rms noise with analog input signal 1 dB below full scale at specified frequency. Tested at 55% duty cycle.
[3]Intermodulation measured with analog input frequencies of 8.9 MHz and 9.8 MHz at 7 dB below full scale.
[4]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.

Specifications subject to change without notice.



AD9022 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ ..... +6 V
$-V_S$ ..... –6 V
Analog Input ..... –1.5 V to +1.5 V
Digital Inputs ..... $+V_S$ to 0 V
Digital Output Current ..... 20 mA
Operating Temperature Range
AD9022AQ/AZ/BQ/BZ ..... –25°C to +85°C
AD9022SQ/SZ ..... –55°C to +125°C
Maximum Junction Temperature[2] ..... +175°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Storage Temperature Range ..... –65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: "Q" Package (Ceramic DIP): θ_{JC} = 10°C/W; θ_{JA} = 35°C/W. "Z" Package (Gullwing Surface Mount): θ_{JC} = 13°C/W; θ_{JA} = 45°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9022AQ/BQ	–25°C to +85°C	28-Lead Ceramic DIP	Q-28
AD9022AZ/BZ	–25°C to +85°C	28-Pin Ceramic Leaded Chip Carrier	Z-28
AD9022SQ	–55°C to +125°C	28-Lead Ceramic DIP	Q-28
AD9022SZ	–55°C to +125°C	28-Pin Ceramic Leaded Chip Carrier	Z-28

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III – Sample tested only.

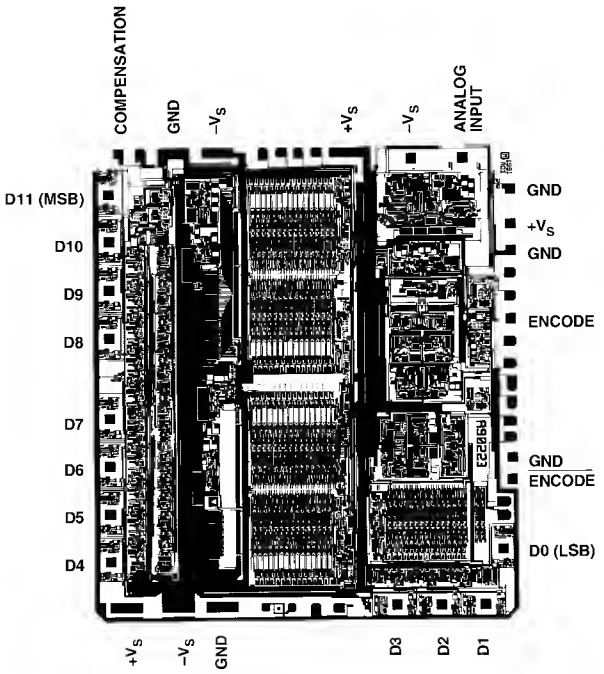
IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; guaranteed by design and characterization testing for industrial devices.

DIE LAYOUT AND MECHANICAL INFORMATION

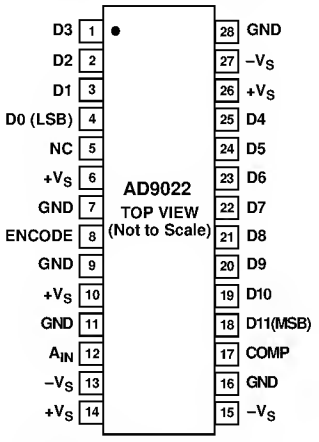
Die Dimensions . . . . . 205 × 228 × 21 (±1) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Transistor Count 4,080
Passivation . . . . . Oxynitride
Bond Wire . . . . . Aluminum



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1–3	D3–D1	Digital output bits of ADC; TTL compatible.
4	D0 (LSB)	Least significant bit of ADC output; TTL compatible.
5	NC	No Connection Internally
6	$+V_S$	+5 V Power Supply
7	GND	Ground
8	ENCODE	Encode clock input to ADC. Internal T/H is placed in hold mode (ADC is encoding) on rising edge of encode signal.
9	GND	Ground
10	$+V_S$	+5 V Power Supply
11	GND	Ground
12	A_{IN}	Noninverting input to T/H amplifier.
13	$-V_S$	–5.2 V Power Supply
14	$+V_S$	+5 V Power Supply
15	$-V_S$	–5.2 V Power Supply
16	GND	Ground
17	COMP	Should be connected to $-V_S$ through 0.1 μF capacitor.
18	D11 (MSB)	Most significant bit of ADC output; TTL compatible.
19–25	D10–D4	Digital output bits of ADC; TTL compatible.
26	$+V_S$	+5 V Power Supply
27	$-V_S$	–5.2 V Power Supply
28	GND	Ground

PIN DESIGNATIONS



NC = NO CONNECT
COMPENSATION (PIN 17) SHOULD BE CONNECTED TO $-V_S$ THROUGH 0.01μF

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Harmonic Distortion
The rms value of the fundamental divided by the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency tested drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the rising edge of the ENCODE command and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 12-bit accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

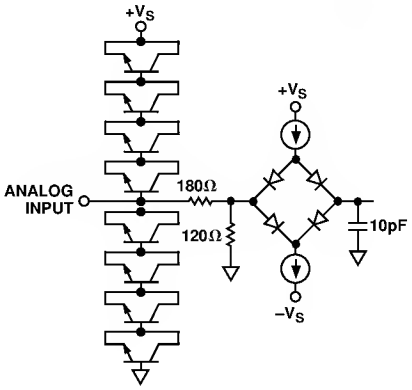
Power Supply Rejection Ratio (PSRR)
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

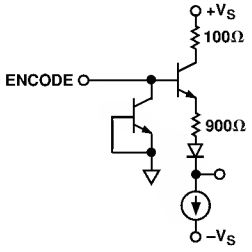
Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, excluding the first five harmonics and dc, with an analog input signal 1 dB below full scale.

Transient Response
The time required for the converter to achieve 12-bit accuracy when a step function is applied to the analog input.

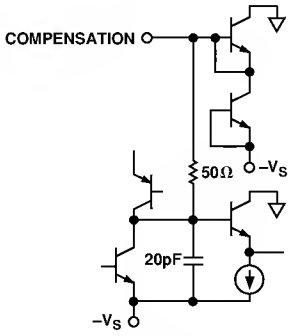
Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.



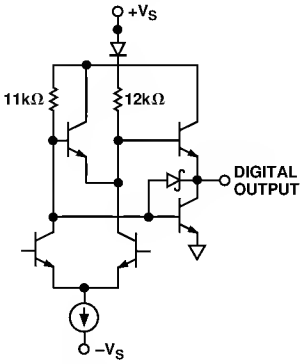
Analog Input



Encode Input



Compensation



Output Stage

Figure 1. Equivalent Circuits

AD9022–Typical Performance Characteristics

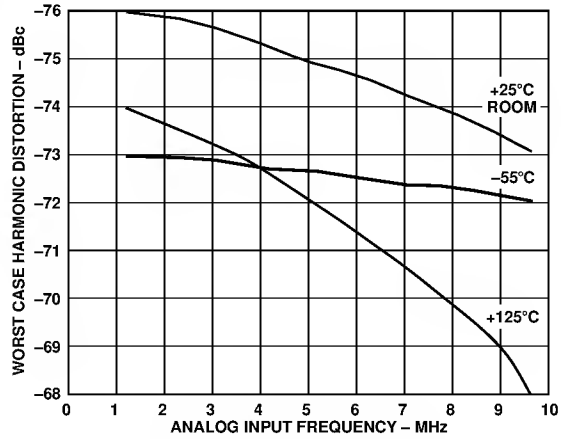


Figure 2. Harmonic Distortion vs. Analog Input Frequency

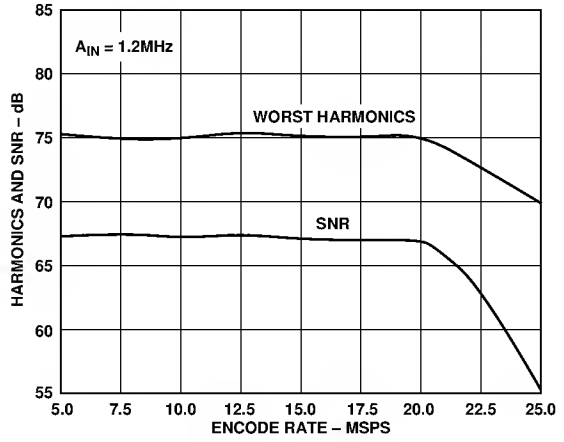


Figure 3. SNR and Harmonics vs. Encode Rate

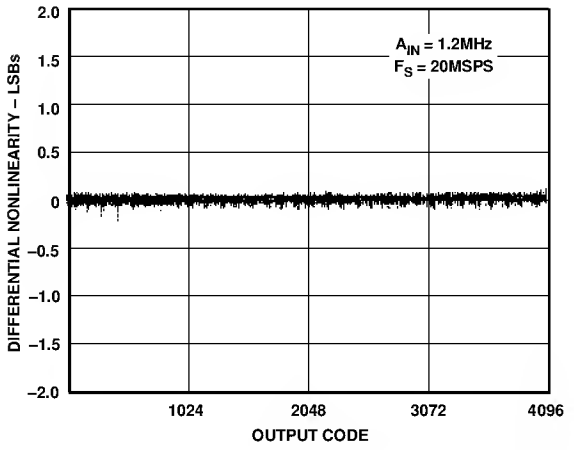


Figure 4. Differential Nonlinearity vs. Output Code

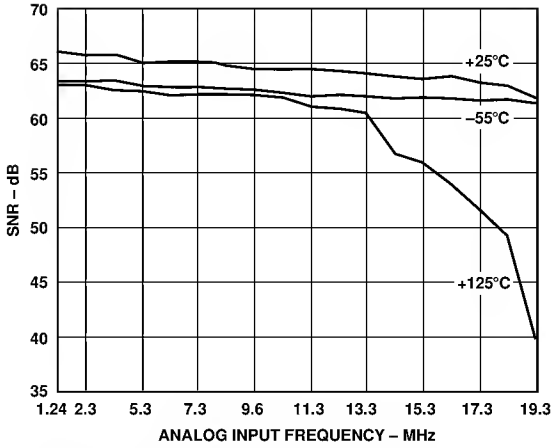


Figure 5. Signal-to-Noise Ratio vs. Analog Input Frequency

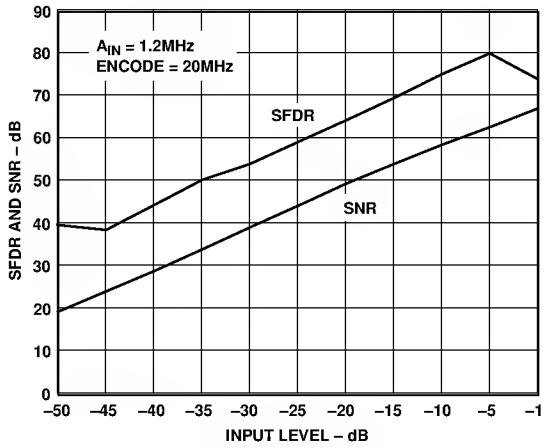


Figure 6. SFDR and SNR vs. Analog Input Level

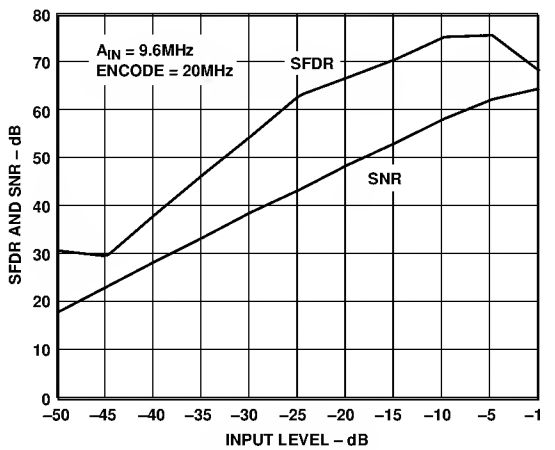


Figure 7. SFDR and SNR vs. Analog Input Level

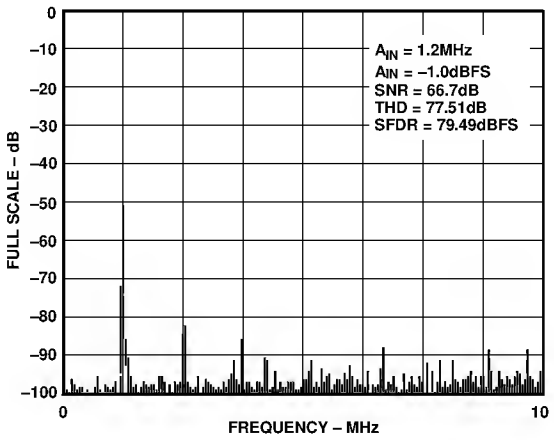


Figure 8. FFT Plot

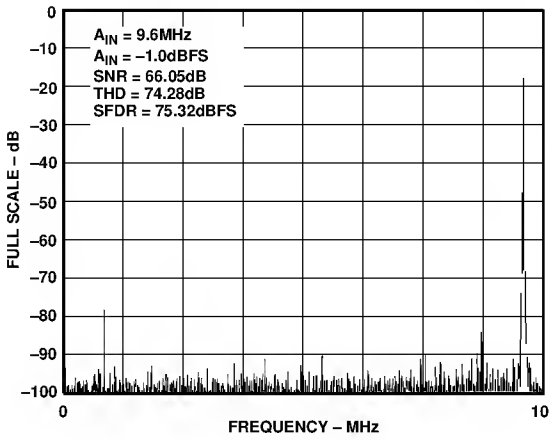


Figure 9. FFT Plot

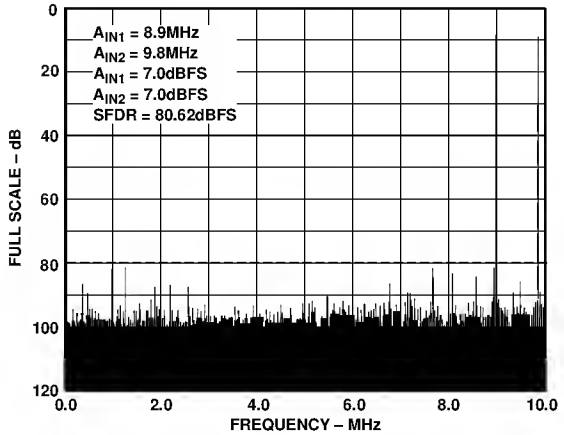


Figure 10. Two-Tone FFT

THEORY OF OPERATION

Refer to the block diagram.

The AD9022 employs a three-pass subranging architecture and digital error correction. This combination of design techniques ensures 12-bit accuracy at relatively low power.

Analog input signals are immediately attenuated through a resistor divider and applied directly to the sampling bridge of the track-and-hold (T/H). The T/H holds whatever analog value is present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse, which should conform to the minimum and maximum pulsewidth requirements shown in the specifications. Operation below the recommended encode rate (4 MSPS) may result in excessive droop in the internal T/H devices–leading to large dc and ac errors.

The held analog value of the first track-and-hold is applied to a 5-bit flash converter and a second T/H. The 5-bit flash converter resolves the most significant bits (MSBs) of the held analog voltage. These five bits are reconstructed via a 5-bit DAC and subtracted from the original T/H output signal to form a residue signal.

A second T/H holds the amplified residue signal while it is encoded with a second 5-bit flash ADC. Again the five bits are reconstructed and subtracted from the second T/H output to form a residue signal. This residue is amplified and encoded with a 4-bit flash ADC to provide the three least significant bits (LSBs) of the digital output and one bit of error correction.

Digital Error Correction logic aligns the data from the three flash converters and presents the result as a 12-bit parallel digital word. The output stage of the AD9022 is TTL. Output data may be strobed on the rising edge of the ENCODE command.

AD9022 IN RECEIVER APPLICATIONS

Advances in semiconductor processes have resulted in low cost digital signal processing (DSP) and analog signal processing which can help create cost effective alternative receiver designs. Today, an all-digital receiver allows tuning, demodulation, and detection of receiver signals in the digital domain. By digitizing IF signals directly, and utilizing digital techniques, it becomes possible to make significant improvements in receiver design. For high frequency IFs, the ADC is the key to the receiver's performance. Unfortunately, the specifications frequently used by receiver designers and analog-to-digital (ADC) manufacturers are often very different. Noise Figure and Intercept Point are common measures of noise and linearity in analog RF system design. ADCs are more frequently specified in terms of SNR and harmonic distortion.

Noise

Noise figure (NF) is a measure of receiver sensitivity and is defined as the degradation of signal-to-noise ratio (SNR) as a signal passes through a device. In equation form:

$$NF = SNR\ (in) - SNR\ (out)$$

Noise figure is a bandwidth invariant parameter for reasonably narrow bandwidths in most devices. The system noise figure for a combination of amplifiers and mixers, for instance, can be analyzed without regard to the information bandwidth.

Thermal noise contribution from the ADC behaves in a similar fashion; however, the spectral density of quantization noise is a function of the sample rate. In addition, the spectral density of the quantization noise is flat only in an ADC with perfect linearity, i.e., perfect 1 LSB step sizes.

To analyze the system noise performance, ADC noise figure is calculated by normalizing the SNR of the ADC output to a 1 Hz bandwidth. This result is given by:

$$SNR\ (/Hz) = SNR + 10\log_{10}(F_S/2)$$

where F_S is the sample rate.

This will be true only for converters in which perfect quantization noise dominates. There may be an upper sample rate, above which the thermal noise of the converter is the dominant source of noise. In this case, normalization would be based on the noise bandwidth of the ADC. For an AD9022 with a typical SNR of 64 dB and a sample rate of 20 MSPS, the normalized SNR is equal to 134 dB (64 + 70). Both thermal and quantization noise contribute to this number.

The SNR of the input is assumed to be limited by the thermal noise of the input resistance, or –174 dBm/Hz. The input signal level is +10 dBm (2 V p-p into 50 Ω). Noise figure of the ADC can be calculated by:

$$NF = SNR\ (in) - SNR\ (out) = [+10 - (174)] - 134 = 50\ dB$$

Most ADCs detect input voltage levels, not power. Consequently, the input SNR can be determined more accurately by determining the ratio of the signal voltage to the noise voltage of the terminating resistor. However, both the input signal and noise voltage delivered to the ADC are also a function of the source impedance. The dependence of NF on sample rate, linearity, source and terminating impedances, and the number of assumptions required, highlight the weakness of using NF as a figure of merit for an ADC. The rather large number that results bolsters this belief by indicating the ADC is often the weakest link in the signal processing path.

Linearity

The Third Order intercept point for a linear device (with some nonlinearity) is a good way to predict 3rd order spurious signals as a function of input signal level. For an ADC, however, this in an invalid concept except with signals near full scale. As the input signal is reduced, the performance burden shifts from the input track-and-hold (T/H) to the encoder. This creates a nonlinear function, as contrasted with the third order intercept behavior, which predicts an improvement in dynamic range as the signal level is decreased.

For signals near full scale, the intercept point is calculated the same as any device:

$$Intercept\ Point = [Harmonic\ Suppression/(N - 1)] + Input\ Power$$

where N = the order of the IMD (3 in this case)

$$AD9022\ Intercept\ Point = 80/2 + 3\ dBm\ (7\ dBm\ below\ full\ scale) = 43\ dBm$$

For signals below this level, the spurious free dynamic range (SFDR) curves shown in the data sheet are a more accurate predictor of dynamic range. The SFDR curve is generated by measuring the ratio of the signal (either tone in the two-tone measurement) to the worst spurious signal, which is observed as the analog input signal amplitude is swept.

The worst spurious signal is usually the second harmonic or 3rd order IMD. Actual results are shown on several plots. The straightline with a slope of one is constructed at the point where the worst SFDR touches the line. This line, extrapolated to full scale, gives the SFDR of the ADC. This value can then be used to predict the dynamic range by simply subtracting the input level from the SFDR.

It should be noted that all SFDR lines are constructed to be valid only below a certain level below full scale. Above these points, the linearity of the device is dominated by the nonlinearities of the front end and best predicted by the intercept point.

AD9022 NOISE PERFORMANCE

High speed, wide bandwidth ADCs such as the AD9022 are optimized for dynamic performance over a wide range of analog input frequencies. However, there are many applications (Imaging, Instrumentation, etc.) where dc precision is also important. Due to the wide input bandwidth of the AD9022 for a given input voltage, there will be a range of output codes which may occur. This is caused by unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to the ADC and several thousand outputs are recorded, a distribution of codes such as that shown in the histogram below may result.

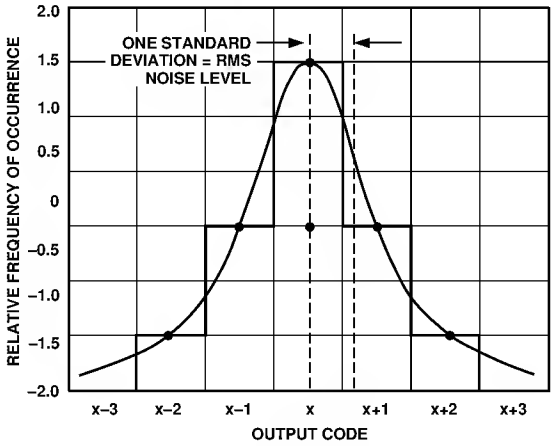


Figure 11. ADC Equivalent Input Noise

The correct code appears most of the time, but adjacent codes also appear with reduced probability. If a normal probability density curve is fitted to this Gaussian distribution of codes, the standard deviation will be equal to the equivalent input rms noise of the ADC. The rms noise may also be approximated by converting the SNR, as measured by a low frequency FFT, to an equivalent input noise. This method is accurate only if the SNR performance is dominated by random thermal noise (the low frequency SNR without harmonics is the best measure). Sixty-three dB equates to 1 LSB rms for a 2 V p-p (0.707 V rms) input signal. The AD9022 has approximately 0.5 LSB of rms noise or a noise limited SNR of 69 dB, indicating that noise alone does not limit the SNR performance of the device (quantization noise and linearity are also major contributors).

This thermal noise may come from several sources. The drive source impedance should be kept low to minimize resistor thermal noise. Some of the internal ADC noise is generated in the wideband T/H. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD9022 has an input bandwidth of over 100 MHz, even though the sampling rate is limited to 20 MSPS.)

Wide bandwidth is required to minimize gain and phase distortion and to permit adequate settling times in the internal amplifiers and T/Hs. But a certain amount of unavoidable noise is generated in the T/H and other wideband circuits within the ADC; this causes variation in output codes for dc inputs. Good layout, grounding and decoupling techniques are essential to prevent external noise from coupling into the ADC and further corrupting performance.

USING THE AD9022

Layout Information

Preserving the accuracy and dynamic performance of the AD9022 requires that designers pay special attention to the layout of the printed circuit board.

Analog paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input connection should be kept away from digital signal paths; this reduces the amount of digital switching noise, which is capacitively coupled into the analog section. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. The AD9022 digital outputs should be buffered or latched close to the device (<2 cm). This prevents load transients that may feed back into the device.

In high speed circuits, layout of the ground is critical. A single, low impedance ground plane on the component side of the board is recommended. Power supplies should be capacitively coupled to the ground plane with high quality 0.1 µF chip capacitors to reduce noise in the circuit. All power pins of the AD9022 should be bypassed individually. The compensation pin (COMP Pin 17) should be bypassed directly to the $-V_S$ supply (Pin 15) as close to the part as possible using a 0.1 µF chip capacitor.

Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance ground planes. In systems with dedicated analog and digital grounds, all grounds for the AD9022 should be connected to the analog ground plane.

In systems using multilayer boards, dedicated power planes are recommended to provide low impedance connections for device power. Sockets limit dynamic performance and are not recommended for use with the AD9022.

Timing

Conversion by the AD9022 is initiated by the rising edge of the ENCODE clock (Pin 8). All required timing is generated internal to the ADC. Care should be taken to ensure that the encode clock to the AD9022 is free from jitter that can degrade dynamic performance. The clock driver should be compatible with TTL LS logic series devices. Drivers with excessive slew rate or overdrive will degrade the dynamic performance of the AD9022.

Pulsewidth of the ADC encode clock must be controlled to ensure the best possible performance. Dynamic performance is guaranteed with a clock pulse HIGH minimum of 25 ns. Operation with narrower pulses will degrade SNR and dynamic performance. From a system perspective, this is generally not a problem, because a simple inverter can be used to generate a suitable clock if the system clock is less than 25 ns wide.

The AD9022 provides latched data outputs. Data outputs are available two pipeline delays and one propagation delay after the rising edge of the encode clock (refer to the AD9022 Timing Diagram). The length of the output data lines and the loads placed on them should be minimized to reduce transients within the AD9022; these transients can detract from the converter's dynamic performance.

Operation at encode rates less than 4 MSPS is not recommended. The internal track-and-hold saturates, causing erroneous conversions. This T/H saturation precludes clocking the AD9022 in a burst mode.

The duty cycle of the encode clock for the AD9022 is critical for obtaining rated performance of the ADC. Internal pulsewidths within the track-and-hold are established by the encode command pulsewidth; to ensure rated performance, minimum and maximum pulsewidth restrictions should be observed. Operation at 20 MSPS is optimized when the duty cycle is held at 55%.

Analog Input

The analog input (Pin 12) voltage range is nominally ±1.024 volts. The range is set with an internal voltage reference and cannot be adjusted by the user. The input resistance is 300 Ω and the analog bandwidth is 110 MHz, making the AD9022 useful in undersampling applications.

The AD9022 should be driven from a low impedance source. The noise and distortion of the amplifier should be considered to preserve the dynamic range of the AD9022.

Power Supplies

The power supplies of the AD9022 should be isolated from the supplies used for noisy devices (digital logic especially) to reduce the amount of noise coupled into the ADC. For optimum performance, linear supplies ensure that switching noise from the supplies does not introduce distortion products during the encoding process. If switching supplies must be used, decoupling recommendations above are critically important. The PSRR of the AD9022 is a function of the ripple frequency present on the supplies. Clearly, power supplies with the lowest possible frequency should be selected.

AD9022 EVALUATION BOARD

The evaluation board for the AD9022 (AD9022/PCB) provides an easy and flexible method for evaluating the ADC's performance without (or prior to) developing a user-specific printed circuit board. The two-sided board includes a reconstruction DAC and digital output interface, and uses the layout and applications suggestions outlined above. It is available at nominal cost from Analog Devices, Inc.

Input/Output/Supply Information

Power supply, analog input, clock connections and reconstructed output (RC OUTPUT) are identified by labels on the evaluation board.

Operation of the evaluation board will conform to the following characteristics:

Parameter	Typical	Units
Supply Current		
+5 V	150	mA
–5 V	300	mA
A_{IN}		
Impedance	51	Ω
Voltage Range	±1.024	V
CLOCK		
Impedance	51	Ω
Frequency	20	MSPS
RC OUTPUT		
Impedance	51	Ω
Voltage Range	0 to –1	V

Analog Input

Analog input signals can be directly fed into the device under test input (A_{IN}). The A_{IN} input is terminated at the device with a 62 Ω resistor to give a parallel equivalent of 51 Ω (62 Ω‖300 Ω).

DAC Reconstruction

The AD9022 evaluation board provides an onboard AD9713B reconstruction DAC for observing the digitized analog input signal. The AD9713B is terminated into 51 Ω to provide a 1 V p-p signal at the output (RC Output).

Output Data

The output data bits are latched with two 74LS574 latches which drive a 40-pin connector (AMP p/n 102153-09). The data and clock signals are available at the connector per the pin assignments shown on the schematic of the evaluation board. Data is latched on the rising edge of the encode clock.

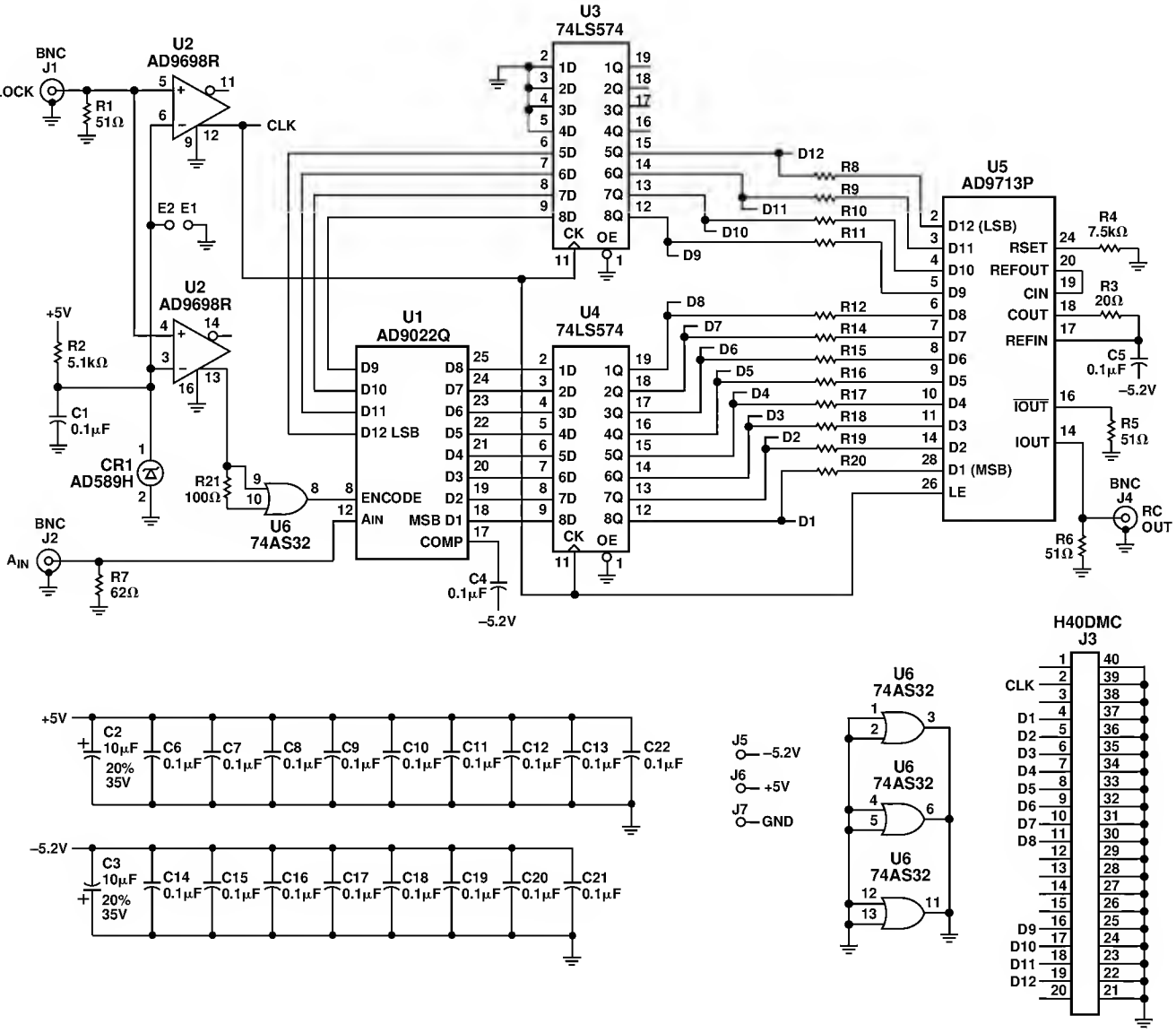


Figure 12. AD9022/PCB Evaluation Board Schematic

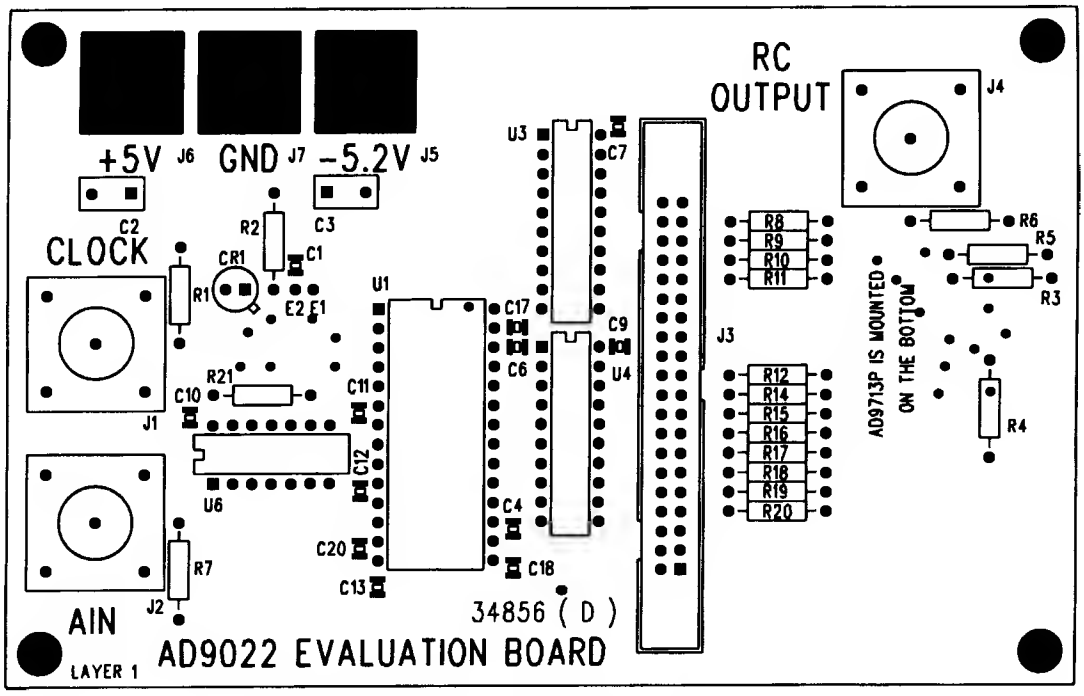


Figure 13. Top of Board, Viewed From Top

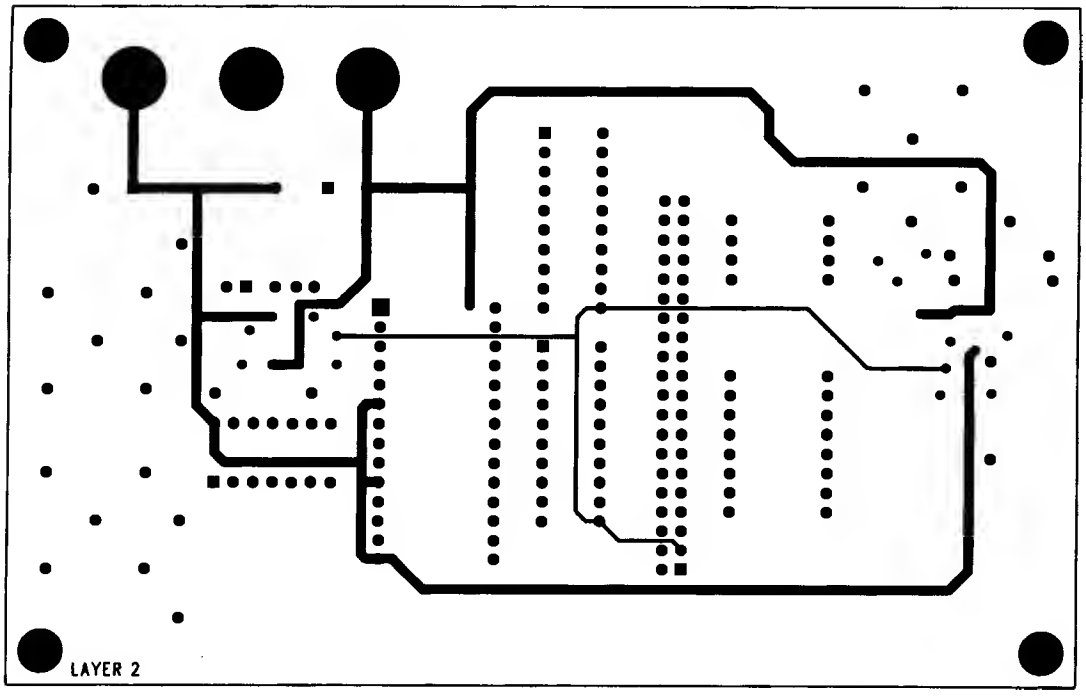


Figure 14. Center of Board, Viewed From Top

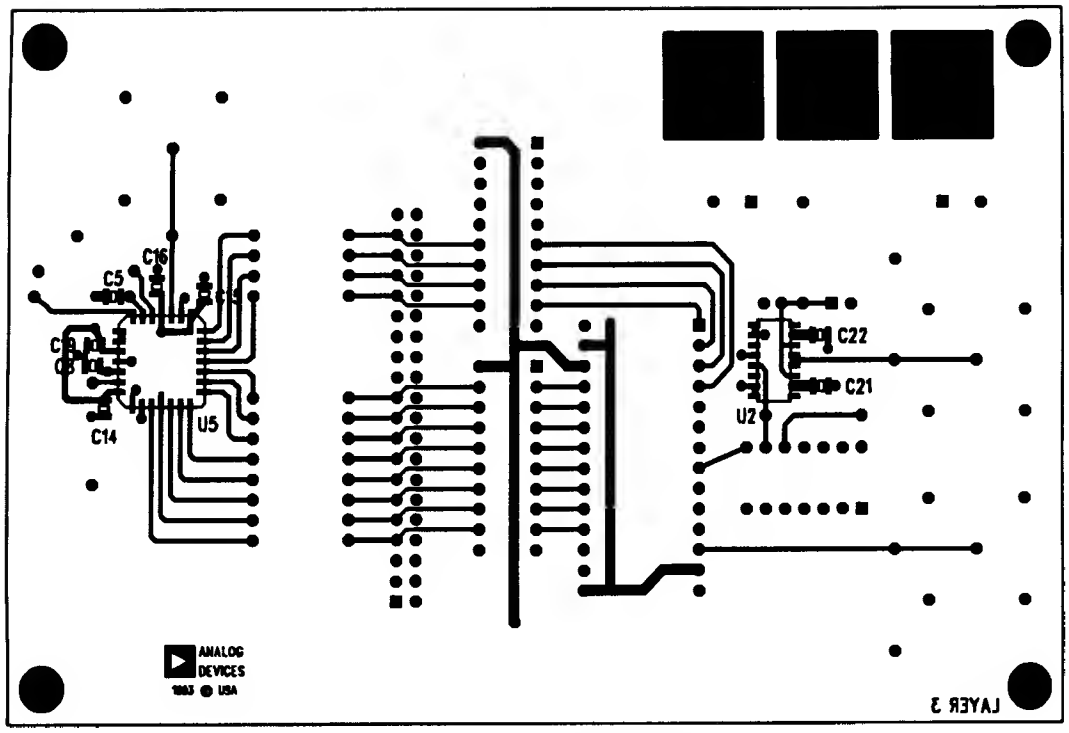
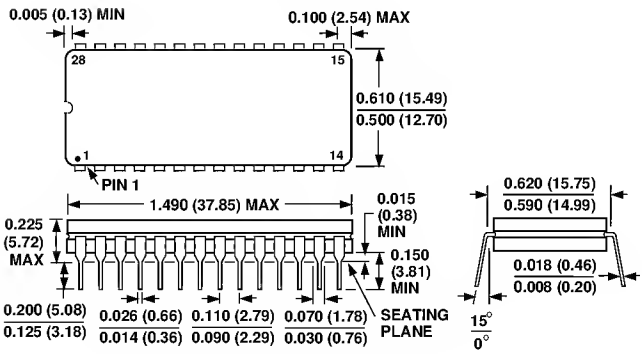


Figure 15. Bottom of Board, Viewed from Bottom

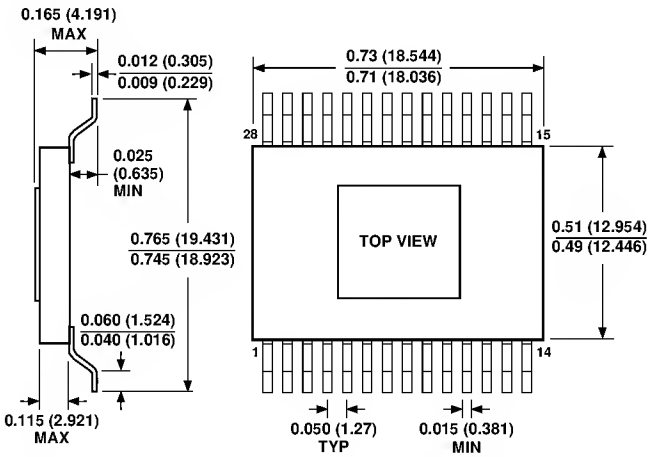
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Cerdip (Q-28)



28-Pin Ceramic Leaded Chip Carrier (Z-28)



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